WHAT IS CLAIMED IS:

1. A transceiver, comprising:

a first interface configured to receive data from a first channel using a first clock signal and to transmit data to the first channel using a second clock signal;

a second interface configured to receive data from a second channel using a third clock signal and to transmit data to the second channel using a fourth clock signal; and

a re-timer configured to re-time data received from the first channel using the first clock signal and to retransmit the data to the second channel using the fourth clock signal.

2. The transceiver of claim 1, wherein

the first channel includes a first clock line for transmission of the first clock signal and a second clock line for transmission of the second clock signal and the second channel includes a third clock line for transmission of the third clock signal and a fourth clock line for transmission of the fourth clocks signal;

the transceiver further comprises:

a first receiver configured to receive data and the first clock signal from the first channel;

a first transmitter configured to transmit data and the second clock signal to the first channel;

a second receiver configured to receive data and the third clock signal from the second channel;

a second transmitter configured to transmit data and the fourth clock signal to the second channel; and

the re-timer is located between the first receiver and the second transmitter and is configured to re-time data received from the second channel using the third clock signal for retransmission, using the second clock signal, onto the first channel.

3. The transceiver of claim 1, wherein data received by the first interface from the first channel using the first clock signal is first data; and the transceiver further comprises isolation logic to prevent the transceiver from transmitting the first data from the first interface to the first channel using the second clock signal.

4. The transceiver of claim 1, further comprising isolation logic to prevent retransmission of data, received from the first channel, to the second channel.

5. The transceiver of claim 1, further comprising latch-up prevention logic to prevent feedback of data between the first and second channels.

6. The transceiver of claim 1, further comprising a first synchronizing unit that synchronizes data transmitted from the first channel to the second channel.

7. The transceiver of claim 6, further comprising a second synchronizing unit that synchronizes data transmitted from the second channel to the first channel.

8. The transceiver of claim 1, wherein the third and fourth clock signals are synchronized to the second clock signal.

9. The transceiver of claim 1, further comprising command interpretation and command performance circuitry.

10. The transceiver of claim 1, wherein the second and forth clock signals are synchronized.

11. A system comprising:

a first channel;

a second channel;

a first device coupled to the first channel;

a second device coupled to the second channel; and

a transceiver having latency aligning circuitry coupled to the first channel and to the second channel.

12. The system of claim 11, wherein at least one of the first and second channels comprises a serial link.

13. The system of claim 12, wherein data transmissions from the first device to the first channel are clocked by a first clock signal and wherein the latency aligning circuitry aligns the round-trip latency between the first device and the second channel to an integer number of cycles of the first clock signal.

14. The system of claim 12, wherein the system has a round trip latency from the first device to the second device that is independent of a flight time from the first device to the second device.

15. The system of claim 14, wherein the latency aligning circuitry is configured to compensate for the flight time from the first device to the second device.

16. The system of claim 12, wherein a first latency, measured by a time required for the transceiver to receive a signal from the first channel and transmit the signal to the second channel, is dependent upon the flight time from the first device to the transceiver.

17. The system of claim 12, wherein the transceiver further comprises isolation logic to prevent retransmission of data, received from the first channel, to the second channel.

18. The system of claim 12, wherein the transceiver further comprises latch-up prevention logic to prevent feedback of data between the first and second channels.

19. The system of claim 12, wherein the transceiver further comprises a first synchronizing unit that synchronizes data transmitted from the first channel to the second channel.

20. The system of claim 19, wherein the transceiver further comprises a second synchronizing unit that synchronizes data transmitted from the second channel to the first channel.

21. The system of claim 12, wherein the transceiver further comprises power logic that turns off the transceiver when the transceiver does not need to transmit.

22. The system of claim 12, wherein data transmissions from the first device to the first channel are clocked by a first clock signal, data transmissions from the transceiver to the first channel are clocked by a second clock signal, data transmissions from the second device to the second channel are clocked by a third clock signal and data transmissions from the transceiver to the second device are clocked by a fourth clock signal.

23. The system of claim 22, wherein the second and fourth clock signals are synchronized.

24. The system of claim 12, wherein the transceiver further comprises at least one phase locked loop that performs clock recovery.

25. A memory system comprising

a memory controller coupled to a primary channel;

a first transceiver, having latency aligning circuitry, coupled to the primary channel and to a first stick channel.

a first memory device having a programmable delay coupled to the first stick channel; and

a second memory device having a programmable delay coupled to the primary channel or the first stick channel.

26. The memory system of claim 25, further comprising a second transceiver having latency aligning circuitry coupled to the stick channel and a second stick channel.

27. The memory system of claim 26, wherein the latency aligning circuitry of the first and second transceivers aligns a respective round-trip latency between the memory controller and each of the transceivers to a respective integer number of clock cycles.

28. The memory system of claim 27, wherein the round-trip latency between the memory controller and the first transceiver is a first integer number of clock cycles and the round-trip latency between the memory controller and the second transceiver is a second integer number of clock cycles and the first and second integer numbers are different.

29. The memory system of claim 26, further comprising a third memory device having programmable delay coupled to the second stick channel.

30. The memory system of claim 29, wherein the first memory device has a first programmed delay, the second memory device has a second programmed delay, the third memory device has a third programmed delay and wherein the first, second and third programmed delays are selected such that response latencies of the first, second and third memory devices are substantially equal.

31. The memory system of claim 25, wherein the first memory device has a first programmed delay and the second memory device has a second programmed delay and wherein the first and second programmed delays are selected such that response latencies of the first and second memory devices are substantially equal.

32. The memory system of claim 25, wherein the transceiver further comprises power logic to power off one or more of the transceivers when such transceivers do not need to transmit.